WHAT IS CLAIMED IS:

1. An analog to digital converter comprising:

a plurality of arrays of autozero amplifiers arranged in series in each array, wherein each autozero amplifier receives an output of a preceding autozero amplifier, wherein a first autozero amplifier in each array amplifiers receives an input signal and a corresponding reference voltage at its inputs, and

wherein at least one of the autozero amplifiers includes a circuit that receives the signal corresponding to the output signal, the circuit substantially passing the signal corresponding to the output signal and the reference voltages to the amplifiers during the clock phase ϕ_2 and substantially rejecting the signal corresponding to the output signal during the clock phase ϕ_1; and

an encoder converting outputs of the autozero amplifiers to an N-bit digital signal representing the input signal.

2. The analog to digital converter of claim 1, further comprising a track-and-hold amplifier tracking the input signal with its output signal during clock phase ϕ_1 and holding a sampled value during the clock phase ϕ_2, the first autozero amplifier in each array receiving its input signal from the track-and-hold amplifier.

3. The analog to digital converter of claim 2, further including a sampling capacitor at each input of the autozero amplifiers for sampling the output of the track-and-hold amplifier.

4. The analog to digital converter of claim 2, wherein the output signal of the track-and-hold amplifier includes positive and negative differential outputs, and

further including a transistor connected between positive and negative differential outputs of the circuit, a gate of the transistor being driven by the clock phase ϕ_1.

5. The analog to digital converter of claim 4, wherein, for each autozero amplifier, the circuit includes two cross-coupled transistors, two signal inputs and two signal outputs, the two signal outputs differentially connected to differential inputs of each corresponding autozero amplifier, the two signal inputs differentially connected to the output signal of the track-and-hold amplifier.

6. The analog to digital converter of claim 4, wherein the circuit includes first, second, third and fourth transistors,

wherein sources of the first and second transistors are connected to a positive differential output of the track-and-hold amplifier through a first sampling capacitor,

wherein sources of the third and fourth transistors are connected to a negative differential output of the track-and-hold amplifier through a second sampling capacitor,

wherein drains of the first and third transistors are connected to a positive differential input of the each autozero amplifier,

wherein drains of the second and fourth transistors are connected to a negative differential input of the each autozero amplifier, and

wherein gates of the second and third transistors are driven by the clock phase ϕ_1.

7. The analog to digital converter of claim 1, wherein, for each autozero amplifier, the circuit includes a plurality of transistors driven by either a supply voltage or the clock phase ϕ_1.

8. The analog to digital converter of claim 1, further including a transistor connected between the positive and negative differential outputs of the circuit, a gate of the transistor being driven by the clock phase ϕ_1.

9. The analog to digital converter of claim 1, further including a transistor connected between the positive and negative differential inputs of the circuit, a gate of the transistor being driven by the clock phase ϕ_1.

10. The analog to digital converter of claim 9, further including:

a first reset transistor connected between a reset voltage and the positive differential output;

a second reset transistor connected between the reset voltage and the negative differential output,

wherein gates of the first and second reset transistors are driven by the clock phase ϕ_1.

11. The analog to digital converter of claim 1, wherein at least some of the autozero amplifiers include a plurality of amplifier stages, and

wherein the circuit is coupled to an input of a first stage of such an autozero amplifier.

12. The analog to digital converter of claim 1, wherein at least some of the autozero amplifiers include a plurality of amplifier stages, and

wherein the circuit is coupled to a first stage of such an autozero amplifier.

13. The analog to digital converter of claim 1, wherein each of the autozero amplifiers includes a plurality of amplifier stages, and

wherein the circuit is coupled to inputs of alternating stages.

14. An analog to digital converter comprising:

a first plurality autozero amplifiers arranged in series, wherein each autozero amplifier receives an output of a preceding autozero amplifier, wherein a first autozero amplifier receives an input signal and a corresponding reference voltage at its inputs, and

wherein at least one of the autozero amplifiers includes a switching circuit that receives the signal corresponding to the output signal and has a differential mode transfer function of approximately 1 on the clock phase ϕ_2 and approximately 0 on the clock phase ϕ_1;

a second plurality of autozero amplifiers inputting the reference voltages and the signal corresponding to the output signal through the switching circuit, the reference voltages selected based on outputs of the first plurality of autozero amplifiers; and

an encoder converting outputs of the first and second plurality of amplifiers to an N-bit digital signal representing the input signal.

15. The analog to digital converter of claim 14, further including a track-and-hold amplifier tracking an input signal with its output signal during a clock phase ϕ_1 and holding a sampled value during a clock phase ϕ_2, wherein a first autozero amplifier in the first plurality of amplifiers receives its input signal from the track-and-hold amplifier.

16. The analog to digital converter of claim 15, further including a sampling capacitor for sampling the output of the track-and-hold amplifier.

17. The analog to digital converter of claim 15, wherein, each autozero amplifier of the second plurality of autozero amplifiers also includes the switching circuit,

wherein the switching circuit includes two cross-coupled transistors, two signal inputs and two signal outputs, the two signal outputs differentially connected to differential inputs of each corresponding autozero amplifier of the second plurality of autozero amplifiers, the two signal inputs differentially connected to the output signal of the track-and-hold amplifier.

18. The analog to digital converter of claim 15, wherein the output signal of the track-and-hold includes positive and negative differential outputs,

wherein the switching circuit includes first, second, third and fourth transistors,

wherein sources of the first and second transistors are connected to a positive differential output of the track-and-hold amplifier through a first sampling capacitor,

wherein sources of the third and fourth transistors are connected to a negative differential output of the track-and-hold amplifier through a second sampling capacitor,

wherein drains of the first and third transistors are connected to a positive differential input of the each autozero amplifier of the second plurality of amplifiers,

wherein drains of the second and fourth transistors are connected to a negative differential input of the each autozero amplifier of the second plurality of autozero amplifiers, and

wherein gates of the second and third transistors are driven by the clock phase ϕ_1.

19. The analog to digital converter of claim 18, further including a transistor connected between the positive and negative differential outputs of the track and hold amplifier, a gate of the transistor being driven by the clock phase ϕ_1.

20. The analog to digital converter of claim 19, further including:

a first reset transistor connected between a reset voltage and the positive differential output;

a second reset transistor connected between the reset voltage and the negative differential output,

wherein gates of the first and second reset transistors are driven by the clock phase ϕ_1.

21. The analog to digital converter of claim 14, wherein the switching circuit includes a plurality of transistors driven by either a supply voltage or the clock phase ϕ_1.

22. The analog to digital converter of claim 14, wherein each autozero amplifier of the second plurality of autozero amplifiers includes a plurality of amplifier stages and the switching circuit, and

wherein the switching circuit is coupled to an input of a first stage for each autozero amplifier of the second plurality of autozero amplifiers.

23. The analog to digital converter of claim 14, wherein each autozero amplifier of the second plurality of autozero amplifiers includes a plurality of amplifier stages and the switching circuit, and

wherein the switching circuit is coupled to inputs of each stage.

24. The analog to digital converter of claim 14, wherein each autozero amplifier of the second plurality of autozero amplifiers includes a plurality of amplifier stages and the switching circuit, and

wherein the switching circuit is coupled to inputs of alternating stages.